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EXAMINER	
CHOW, CHIH CHING	
ART UNIT	**PAPER NUMBER**
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/043,474	BARAZ ET AL.	
	Examiner	Art Unit	
	Chih-Ching Chow	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/7/07.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8,10-17 and 19-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,10-17 and 19-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 April 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to amendment dated June 7, 2007.

2. Per Applicants' request, claims 1, 10, and 19 have been amended.

3. Claims 1-8, 10-17, and 19-26 remain pending.

Response to Amendment

4. Applicants' amendment filed on 6/7/07, responding to the 1/5/07 Office action provided in the 35 USC § 112 rejections for claims 1-8, 10-17, 19-26. The examiner has reviewed the amended claims 1, 10, and 19 respectfully. The rejection to the 35 USC § 112 rejections is hereby withdrawn in view of Applicants' amended claims 1, 10, and 19.

Response to Arguments

5. The Affidavits submitted on 6/7/07 have been fully considered. Applicant's arguments in regard to the prior art Markstein, see REMARKS pp. 9-10 filed on 6/7/2007, with respect to claims 1-2, 4-8, 10-11, 13-17, 19-20, 22-26 rejections have been considered and are persuasive, therefore rejections of 35 USC § 103 (a) Markstein in view of Langford, and Markstein in view of Langford, further in view of Austin have been withdrawn. However, claims 1-8, 10-17, and 19-26 are not in condition for allowance for the reasons listed hereinafter.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 4-8, 10-11, 13-17, 19-20, 22-26 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,926,646, by Pickett et al., (hereinafter "Pickett").

CLAIM	Pickett
1. A machine-implemented method comprising: analyzing one or more instructions of a first program; and modifying the first program to expand a register set for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set, wherein the one or more registers of an expanded register set ~~for use when executing the first program~~ are used by a second program to store data used to analyze the execution of the first program.	Pickett teaches the feature of expanding a register set. See Pickett's Abstract "A microprocessor includes **an expanded set of registers** in addition to the architected set of registers specified by the microprocessor architecture employed by the microprocessor. The **expanded set of registers are memory-mapped within the context of the program being executed**. (*expanding a register set*)", and further "The implemented portion of the **expanded registers** are accessed as register accesses, while the unimplemented portion are converted to memory accesses. The **decode unit within the microprocessor may be configured to convert instructions** which are coded to access the unimplemented **expanded registers into memory operations to access the corresponding memory location**." --*the decoding process is considered as analyzing one or more instructions of a program*. For 'modifying first program' feature see Pickett's column 2, lines 56-60, "An application program **may make use of the expanded registers** by assigning the most-often used operands in the program to the set of memory locations corresponding to the expanded registers. The application programmer may than **code instructions which access these operands** with **register identifiers corresponding to the expanded** registers." And column 2, lines 43-55, "The microprocessor includes an **expanded set of registers** in addition to the architected set of registers specified by the microprocessor architecture employed by the microprocessor. **The expanded set of registers are memory-mapped within the context of the program being executed**.

Upon a context switch, the microprocessor **saves the state of the expanded registers to the corresponding memory locations**. Advantageously, the context save area defined by the microprocessor architecture is not modified by adding the provided registers. Additionally, since the microprocessor manages the **save and restore of the expanded registers upon context switches**, the addition of the expanded registers is **transparent to operating system software**".– *modifying the program and transparently to execution of the program.* For using expanded registers by a second program feature see Pickett's column 2, lines 25-28, "As used herein, **a context switch** is an event in which one context, corresponding to a **first program, is replaced within the microprocessor by another context corresponding to a second program**".

2. The method of claim 1, comprising:
identifying one or more register moves for the expanded register set; and
modifying the program to perform the first identified one or more register moves.

Claim 1 rejection is incorporated. Further see Pickett's Abstract, "The application programmer may than code instructions which access these operands with **register identifiers corresponding to the expanded registers**. (*identifying one or more registers*)." See claim rejection 1 has for 'modifying program' feature.

4. The method of claim 1, wherein the modifying the first program comprises modifying the first program to expand a register set for a callee routine of the first program.

Claim 1 rejection is incorporated. Further, see Pickett's column 17, lines 19-29, "An additional consideration in the use of instruction redefinition by the application program is the use of operating system routines by the application program. It is desirable to allow instruction redefinition to be utilized by the application program, but to disable instruction redefinition when the operation system executes. In this manner,

	microprocessor 10 may employ instruction redefinition without requiring the operating system to be rewritten. Particularly, if privileged instructions are selected as redefinable instructions, the operating system may need to execute the privileged instruction within the **called operating system routine.**" And column 17 lines 30-34, "Disabling instruction redefinition mode upon context switches effects the disablement of instruction redefinition mode when the operating system begins executing via a context switch. However, **application programs often call operating system service routines**." – the operating system routine is considered as a callee routine, to expand a register for a callee routine of the first program.
5. The method of claim 4, comprising: modifying the first program to expand a register set for a caller routine that is to call the callee routine.	Claim 4 rejection is incorporated. See Pickett's disclosure cited in claim 4 rejection, it covers both callee routine and caller routine, and the caller routine can call the callee routine.
6. The method of claim 5, wherein the modifying the first program to expand a register set for the callee routine comprises modifying the first program to expand a register set that includes one or more registers of the register set for the caller routine.	Claim 5 rejection is incorporated , further see claim 4 rejection.
7. The method of claim 5, comprising: (a) identifying one or more register moves for the register set of the caller routine; and (b) modifying the first program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine.	Claim 5 rejection is incorporated , further see claim 1 rejection.

8. The method of claim 5, comprising:
(a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and
(b) modifying the first program to perform the identified register move.

Claim 5 rejection is incorporated , further see claim 1 rejection.

10. A machine-readable medium having instructions that, if executed by a machine, cause the machine to perform a method comprising:
analyzing one or more instructions of a first program; and
modifying the first program to expand a register set for a routine in the first program transparently to execution of the first program that includes adding one or more registers to the register set, wherein the one or more registers of an expanded register set ~~for use when executing the first program~~ are used by a second program to store data used to analyze the execution of the first program.

Claim 5 rejection is incorporated , further see claim 1 rejection.

Pickett's teaching also covers a machine-readable medium having instructions, see Pickett's claim 33. Claim 10 is a machine-readable version of claim 1, therefore see claim 1 rejection.

11. The machine-readable medium of claim 10, wherein the method comprises:
identifying one or more register moves for the expanded register set; and
modifying the first program to perform the identified one or more register moves.

13. The machine-readable medium of claim 10, wherein the modifying the first program comprises modifying the first program to expand a register set for a callee routine of the first program.

Claim 10 rejection is incorporated , further see claim 2 rejection.

14. The machine-readable medium of claim 13, wherein the method comprises:
modifying the first program to expand a

register set for a caller routine that is to call the callee routine.

Claim 5 rejection is incorporated , further see claim 1 rejection.

15. The machine-readable medium of claim 14, wherein the modifying the first program to expand a register set for the callee routine comprises modifying the first program to expand a register set that includes one or more registers of the register set for the caller routine.

Claim 5 rejection is incorporated , further see claim 1 rejection.

16. The machine-readable medium of claim 14, wherein the method comprises:
(a) identifying one or more register moves for the register set of the caller routine; and
(b) modifying the first program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine.

Pickett's teaching also covers a machine-readable medium having instructions, see Pickett's claim 33. Claim 10 is a machine-readable version of claim 1, therefore see claim 1 rejection.

17. The machine-readable medium of claim 14, wherein the method comprises:
(a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and
(b) modifying the first program to perform the identified register move.

19. A system comprising:
a processor to execute instructions; and
a medium having instructions to analyze one or more instructions of a first program and to modify the first program to expand a register set for a routine in the first program transparently to execution of the program that includes adding one or more registers to the register set, wherein the one or more registers of an expanded register set ~~for use when executing the first program~~ are used by a second program to store data used to

Claim 10 rejection is incorporated , further see claim 2 rejection.

analyze the execution of the one or more instructions of the first program.	Claim 10 rejection is incorporated , further see claim 4 rejection.
20. The system of claim 19, the medium having instructions to identify one or more register moves for the expanded register set and to modify the first program to perform the identified one or more register moves.	Claim 13 rejection is incorporated , further see claim 5 rejection.
22. The system of claim 19, the medium having instructions to modify the first program to expand a register set for a callee routine of the first program.	Claim 14 rejection is incorporated , further see claim 6 rejection.
23. The system of claim 22, the medium having instructions to modify the first program to expand a register set for a caller routine that is to call the callee routine.	
24. The system of claim 23, the medium having instructions to modify the first program to expand a register set that includes one or more registers of the register set for the caller routine.	For the feature of claim 14 see claim 14 rejection. For the rest of the claim 16 feature see claim 7 rejection.
25. The system of claim 23, the medium having instructions to identify one or more register moves for the register set of the caller routine and to modify the first program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine.	Claim 14 rejection is incorporated , further see claim 8 rejection.
26. The system of claim 23, the medium having instructions to identify a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine and to modify the first program to perform the identified register move.	Claim 19 is a system version of claim 1, therefore see claim 1 rejection.

Claim 19 rejection is incorporated , further see claim 2 rejection.

Claim19 rejection is incorporated , further see claim 4 rejection.

For the feature of claim 22 see claim 22 rejection. For the rest of the features see claim 5 rejection.

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 6 rejection.

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 7 rejection.

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 8 rejection.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,926,646 by Pickett et al., (hereinafter "Pickett"), in view of U.S. Patent No. 5, 644,709 by Todd Michael Austin (hereinafter "Austin").

CLAIM	Pickett /Austin
3. The method of claim 2, wherein the identifying comprises: (a) defining one or more move chains for the expanded register set, and (b) identifying a sequence of one or more register moves based on the defined one or more move chains.	For the feature of claim 2 see claim 2 rejection. Pickett teaches all aspects of claim 3, but he does not mention 'move chain' specifically, however, Austin teaches it in an analogous prior art. In Austin column 7, lines 19-26, "A **call-chain** is the state of the stack at some point in a program's execution; it is composed of **a sequence of function names**; functions higher in the **call-chain** call (possibly indirectly) the functions lower in the call **chain**; neighbors in the **call-chain** share a direct **caller-callee relationship**. A partial **call-chain** is a subset of the current complete call-chain, usually taken from the bottom of the complete call chain; partial

	call-chains are usually employed to reduce storage requirements." It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Pickett's disclosures of the analyzing program and expanding registers by call chain taught by Austin, for the purpose of adjusting the appropriate counts at calls (Austin column 7, lines 34-35) thus no callee routine would be left out during a program rearrangement.
12. The machine-readable medium of claim 11, wherein the identifying comprises: (a) defining one or more move chains for the expanded register set, and (b) identifying a sequence of one or more register moves based on the defined one or more move chains.	Claim 11 rejection is incorporated , further see claim 3 rejection.
21. The system of claim 20, the medium having instructions to define one or more move chains for the expanded register set and to identify a sequence of one or more register moves based on the defined one or more move chains.	Claim 20 rejection is incorporated , further see claim 3 rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Christie, US Patent No. 6,877,084, discloses a central processing unit (CPU) is described including a register file and an execution core coupled to the register file. The register file includes a standard register set and an extended register set. The standard register set includes multiple standard registers, and the extended register set include multiple extended registers.

Galbi et al., US Patent No. 6,822,959, discloses Circuitry to free the core processor from performing the explicit read operation required to read data into the internal register set. The processor's register set is expanded and a "shadow register" set is provided.

Worrell et al., US Patent No. 6,412,066, discloses a microprocessor is configured to fetch a compressed instruction set which comprises a subset of a corresponding non-compressed instruction set. The compressed instruction set is a variable length instruction set including 16-bit and 32-bit instructions. The 32-bit instructions are coded using an extend opcode, which indicates that the instruction being fetched is an extended (e.g. 32 bit) instruction. The compressed instruction set further includes multiple sets of register mappings from the compressed register fields to the decompressed register fields.

Le et al., US Patent No. 6,243,668, discloses method of executing a program compiled for a base instruction set architecture different than a native instruction set architecture, on a native machine by organizing a runtime system module into at least a low level domain, a medium level domain, and a high level domain. A memory buffer referred to as a backing store is created to correspond to a register stack and have a one-to-one mapping with the register stack.

11. The following summarizes the status of the claims:

35 USC § 102 rejection: Claims 1-2, 4-8, 10-11, 13-17, 19-20, 22-26

35 USC § 103 rejection: Claims 3, 12, 21

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the **TC2100 Group receptionist: 571-272-2100**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow
Examiner
Art Unit 2191
August 3, 2007

CC

WEI ZHEN
SUPERVISORY PATENT EXAMINER